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Full-thickness Backside Circuit Editing for ASICS on Laminated Packages

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The traditional backside circuit editing strategy on flip chip semiconducting parts comprises approximately 30 min of de-soldering to remove the capacitors and 60 min of polishing to remove 600 μm of bulk Si in preparation for the focused ion beam. Flip chip parts mounted on laminated ball grid array packages have the horrible tendency to crack when polished on a polishing wheel to remove the bulk Si. The formation of cracks has driven the need for a full-thickness backside circuit editing strategy. The authors present a description of the full-thickness backside circuit editing strategy on laminated substrates used for 90/65/40 nm circuit edit work on advanced ASIC circuits at Avago Technologies. In contrast to a part thinning strategy, removal of 600 μm of bulk Si with XeF_2-enhanced trenching eliminates the removal of capacitors, the polishing step, and the need for functional testing. The time to remove 600 μm of bulk Si with XeF_2-enhanced etching is approximately 150 min, making a full-thickness backside circuit editing process competitive with the traditional backside circuit editing process.

Keywords electronic materials, microelectronic failure analysis, modification

1. Introduction

The focused ion beam (FIB) is a valuable tool for semiconductor circuit editing (Ref 1). Rue et al. have presented an article on full-thickness backside circuit edits (Ref 2). ASICs from Avago Technologies are fraught with the same problems and issues described in that manuscript—cracking, thinning, coarse navigation, trenching speed, and secondary emission from a deep hole. A nefarious problem is simply cracking of thinned parts mounted on laminated, organic substrates such as SLC™ packages. Thinned parts have less mechanical strength and are more likely to crack than full-thickness parts. Expensive ceramic packages provide adequate support for thinned flip chip parts, but SLC™ laminated packages are insufficient to prevent cracking during the polishing process or functional testing. This problem mandates the development of a competitive full-thickness backside circuit edit process for work in the 90/65/40 nm technology arenas.

The commonly used FIB technique for backside circuit edits on flip-chip parts that have already been packaged and are ready for shipment requires the removal of the protective lid and capacitors on the package followed by thinning the die on a polishing wheel to remove the bulk of the Si substrate wafer. The final thickness of the remaining Si is not particularly important and is at the discretion of the FIB operator. With care one can thin down to 40 μm although a more typical thickness is greater than 100 μm.

Thinning enables the FIB operator to perform edits quickly but presents several problems. First, the removal of the package capacitors opens key questions for the designers at Avago Technologies, a company offering SerDes ASICs where the primary components are analog. Any change in performance of the device after the FIB edit could in principle result from the removal of the capacitors. The appearance of jitter after a FIB circuit edit is an example.

Heat dissipation is another concern. Designers frequently wish to exercise parts up to and beyond the target temperature demanded by the end user. Thinning from 770 μm down to 100 μm has poorly quantified effects on device performance. Thermal runaway, a potential problem looming in the future, should be worse for thinned die than full thickness die.

This article presents a description of a full-thickness backside edit process, the standard process offered at Avago Technologies. The process uses only the standard recipes on the FEI Company Vectra Vision FIB with some attention for optimization, but otherwise has no special tricks or proprietary concepts.

2. Experimental

The parts for these particular experiments were manufactured at the Taiwan Semiconductor Manufacturing Company with 90, 65, and 40 nm copper technology and mounted on Kyocera SLC™ packages. The thickness of the bulk Si is approximately 770 μm, and chip sizes vary from as small as 4 mm by 4 mm up to 20 mm by 20 mm. All SLC™ packages passed warpage specification of 8 mils (200 μm) center to edge.

The flip chips parts were prepared by prying off the lid with a razor blade. Full-thickness backside edit parts were ready for insertion into the FIB after cleaning with acetone and isopropyl

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alcohol. Thinned parts normally require removal of capacitors with a solder gun and thinning on an Allied Techprep polisher using 30 μm polishing paper for coarse polishing, decreasing the grit to 1 μm for the final polish. The polishing step was skipped entirely.

The VisIon column of the Vectra Vision FIB uses a Ga liquid metal ion source to create a 50 KeV Ga^+ ion beam in the range 15.4 nA down to 5.8 pA. Available gas chemistries for gas-enhanced etching include XeF_2, Cl, and H_2O. In addition to a pentanozzle used for gas delivery, the Vectra VisIon system has a beehive used to concentrate the XeF_2 on the sample surface for increased etching rates. All gas and milling parameters were entered manually, not using the automated recipes in the system software.

The Vectra VisIon system includes a Merlin near infrared (NIR) camera from FLIR equipped with an InGaAs focal plane array detector operating between 0.9 and 1.7 μm. The objective lens is an Olympus LMPlan IR with a 3 mm working distance. The 770 μm thick Si substrate is transparent in this IR region, allowing coarse navigation to the desired worksite and measurement of the trenching depth to an accuracy of 2 μm with a procedure referred to here as "tagging." A tag embodied by a square typically 5 μm on a side is drawn on the bottom of a trench with the 0.1 $nC/\mu m^2$ dose for 2 s. The exact dose and size are not critical. The idea is to create a tag of embedded Ga that reflects infrared radiation and allows focusing of the trench bottom to a precision of 2 μm.

Figure 1(a), (b), and (c) shows a 5 by 5 μm tag in a 70 by 70 μm trench made by dosing with 0.1 $nC/\mu m^2$ of the Ga^+ beam, in and out of focus by ±5 μm. The embedded Ga in the tag reflects NIR radiation so that it appears as a bright spot in the image. By keeping the tagging dose low, subsequent trenching with XeF_2 removes all traces of the tag and prevents the formation of leader-holes that open to the active area before the remainder of the trench.

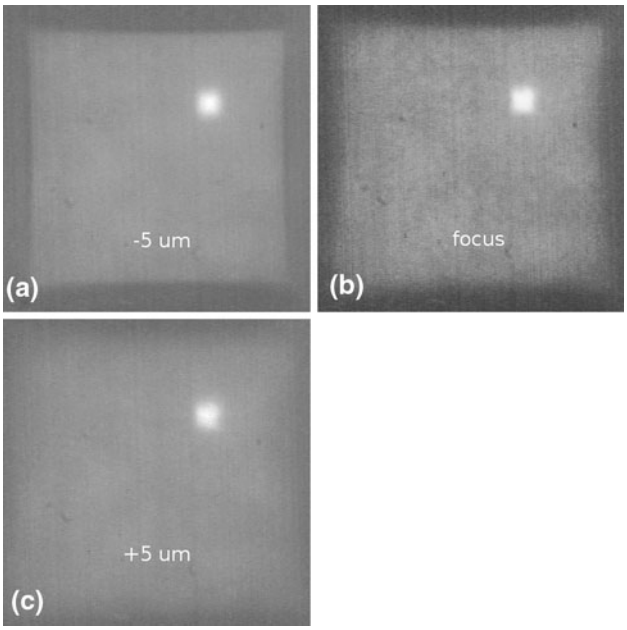

Fig. 1 Tag in a 70 by 70 μm trench, (a) out of focus by +5 μm, (b) in focus, and (c) out of focus by −5 μm

3. Results and Discussion

3.1 Cracking of Thinned 65 nm Chips on Laminated Packages

ASICs mounted on ceramic packages rarely if ever present cracks. Only on laminated, SLC™ packages is cracking a serious problem. Cracking is not a phenomenon relegated only to large die though. Small die seem to be just as susceptible to crack formation during the polishing process.

Figure 2 shows an optical image of cracks that form during the polishing step. The figure shows a 4 mm by 4 mm die mounted on a 25 by 25 mm laminated package 1.4 mm in thickness. The die was thinned to 200 μm by the removal of approximately 570 μm of bulk Si.

The thinned die has two large cracks, one in the lower left propagating down to the right, and one seen as an arc along the right side. The straight lines rising upwards to the right are scratches left from the polishing process. The scratches are difficult to remove because particles of Si chip off of the edges of the die to cause scratches. Figure 3 shows a magnified portion of Fig. 2 in the lower left corner, where cracks along

Fig. 2 4.0 by 4.0 mm die with two cracks

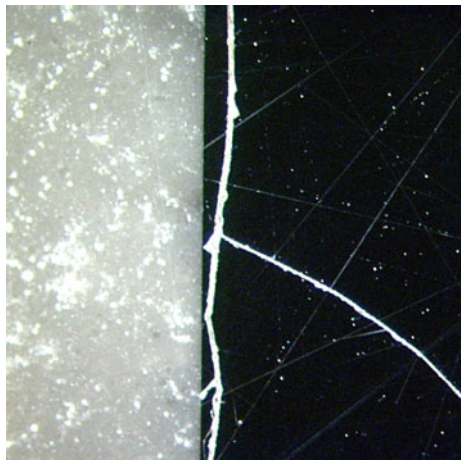

Fig. 3 Lower left corner of the 4.0 by 4.0 mm die

the perimeter of the die that act as a source for large Si particles to scratch the die during the polishing process are clearly evident.

In the worst of cases, cracks form almost instantaneously on the polisher, after the removal of only tens of microns of material. Some parts, on the other hand, polish without cracking down to tens of microns, evincing the straightforward conclusion that the polishing process is unreliable and unpredictable on laminated parts, some working well and others not without a clear forecasting metric.

3.2 Cross Sections of Full-thickness Backside Trenches

Figure 4 shows a trench made in Si by etching for 60 min with the beehive but without a beam. The reservoir pressure was set to 1.3 Torr and the chamber pressure rose to 1.3×10^{-5} Torr. XeF_2 etches Si to produce a number of Si-F products including SiF_4, Si_2F_6, and SiF_3 (Ref 3). The dominant exothermic reaction is

$$Si(s) + 2XeF_2(g) \rightarrow 2Xe(g) + SiF_4(s),$$

The measured Si removal rate for the first hour when the reservoir pressure is set to 1.3 Torr was 2.55 μm/min.

It should be possible to deduce the pressure in the beehive from the etch rate, noting that the etch rate is linear with XeF_2 pressure in a large range from 10^{-8} to 0.5 Torr (Ref 3, 4). However, most experimental data for the etch rate versus pressure were taken under static conditions with a defined pressure (1 Torr) of XeF_2 in an expansion chamber for a set time interval (60 s) (Ref 5-8). In a static environment, the etch rate decreases rapidly as a function of time as XeF_2 near the Si surface is replaced with Xe and SiF_4. Most authors tend to quote the average etch rate in the range of 1-5 μm/min/Torr for the first 60 s of static etching (Ref 5-8). Since the flow conditions of the beehive lead to a constant replacement of the XeF_2 etchant, the etch rate for the conditions of Fig. 4 should mimic the initial etch rate for these static conditions. For the first 10-15 s of etching in a static environment, Winters et al. report 50 μm/min/Torr, Chu et al. report 45 μm/min/Torr, and Sugano et al. report 60 μm/min/Torr (Ref 4, 5, 7). Using an average of 52 μm/min/Torr leads to an estimate of 49 mTorr for the pressure in the beehive.

The pressure of 49 mTorr in the beehive is interesting since it is near the cross-over between laminar flow and molecular flow in the beehive. Statistical physics allows one to compute the mean free path l for a molecule in a gas given a molecular density n and a cross section of σ_o (Ref 9),

$$l = 1/(n\sigma_o\sqrt{2}).$$

The cross-sectional area of XeF_2 is on the order of 2.3×10^{-19} m^2, comprising an area of 5.8×10^{-20} m^2 for the F^- atoms and 1.1×10^{-19} m^2 for the Xe^{2+} atom. The molecular density is

$$n = p/kT,$$

where Boltzmann's constant k is 1.38×10^{-23} m^2 kg/(s^2 K), p is the pressure, and T is the temperature in Kelvin. Combining yields a mean free path of 2.0 mm, comparable to the dimensions of the beehive.

Figure 5 shows a polished cross section of a 100 μm by 100 μm full-thickness backside trench in a 65 nm Si circuit milled with the beehive using the gas conditions of Fig. 4 (1.3 Torr in the reservoir), a 4.4 nA beam, a pixel spacing (px and py) of 0.4 μm, and a pixel dwell time of 0.5 μs. The pattern loop time is defined as the number of pixels in the raster pattern times the dwell time per pixel, which is 32 ms for this pattern (Ref 2). Harriott et al. refer to the pixel dwell time as t_p and the pattern loop time as the pattern refresh time, t_r (Ref 10).

The profile of the trench shows two clear regions. From the top surface of the Si to a depth of 331 μm, one can see an isotropically etched trench made solely by the exothermic reaction between the XeF_2 etch gas and the Si substrate. Below the isotropically etched region is an anisotropic region created by the beam and XeF_2 etchant working in tandem. For the particular mix of beam and pressure used for this trench, the trench shape is conical as shown in Fig. 5.

3.3 Parameters for Trenching Rates with a Ga^+ Beam

Figure 6 shows the trenching rate for four different trenches made with a 4.4 nA beam rastering 100 by 100 μm with px = 0.4 μm, py = 0.4 μm, t_p = 0.5 μs, and t_r = 32 ms. The gas pressure in the reservoir was set to 1.3 Torr and, as deduced previously, the beehive pressure was 49 mTorr. The depths are measured with the NIR microscope using the tagging procedure described in the earlier.

The trenching rate for these conditions starts at 9 μm/min and falls to 5 μm/min near the end of the trench with a 20% variation from run-to-run. The variation stems from the quality of the seal between the Si substrate and the beehive, and can exceed the 20% seen in Fig. 6. At least two phenomena contribute to the decrease in etch rate: (1) as the seal between

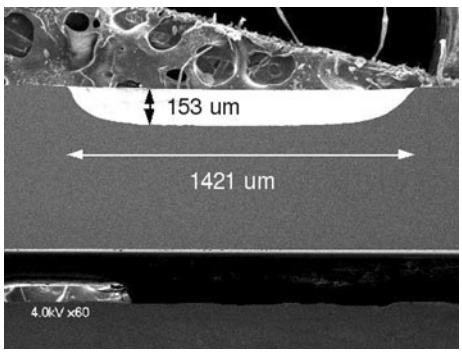

Fig. 4 Polished cross section of a trench made without a beam, using XeF_2 only

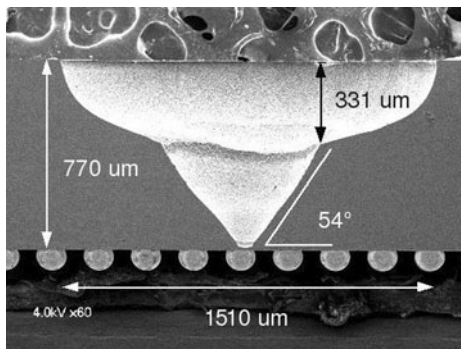

Fig. 5 Polished cross section of a full thickness trench

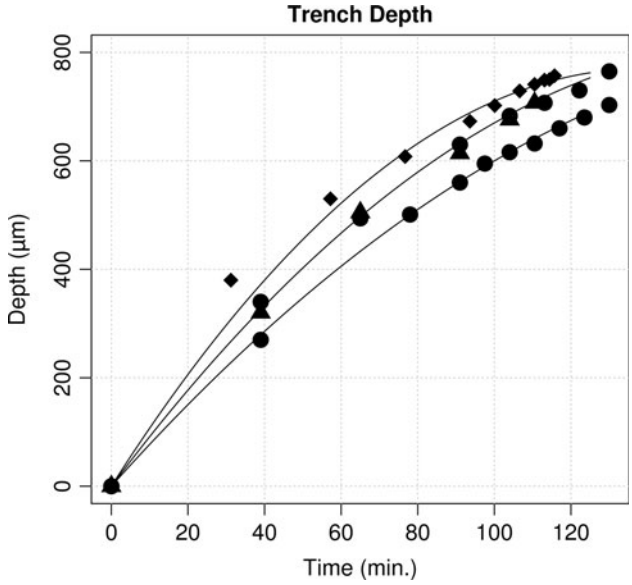

Fig. 6 Trenching depth vs. time

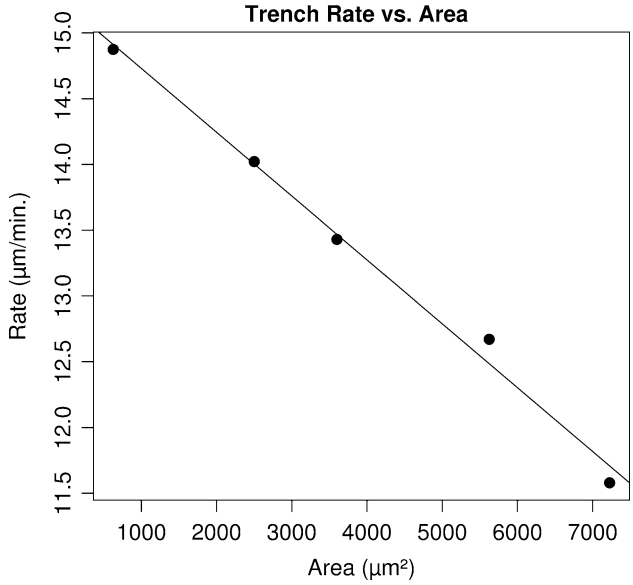

Fig. 7 Trenching rate vs. area

the beehive and the Si surface erodes, more XeF_2 escapes from the beehive, and (2) the surface area of the Si increases with depth as the length of the sidewalls increase. The first effect will lead to a decrease in total pressure in the beehive, and the second will cause a decrease in XeF_2 partial pressure.

One can see from Fig. 6 that the first 70 min of etching removes 500 μm of material, leaving only 270 μm left of the original 770 μm bulk Si. Since removing package capacitors and polishing to a thickness of 270 μm requires an hour or more, this data bust the myth that full-thickness backside circuit edits take too much time. The time saved by not removing capacitors and polishing accounts for the bulk of the extra time required to trench through 770 μm of bulk Si.

The total time to trench to the worksite in Fig. 5 was 3 h with the inclusion of intentional slow trenching near the end to avoid destroying active areas and the employment of leader holes (Ref 2). The trenching rate can be decreased to an arbitrary value by decreasing the gas pressure and the beam current. The information in Fig. 4 and 6 suffices to estimate that the isotropic component to the trenching rate should be 2.55 μm/min for the first hour, slow to 1.91 μm/min during the second hour, and slow to 1.27 μm/min for the third hour. After 2.5 h, the isotropic part of the trench should have a depth of 306 μm as seen in Fig. 5.

3.4 Methods to Increase the Trenching Rate

Harriott et al. have presented a language to describe the scanning parameters used for FIB induced gas etching (Ref 10). Four parameters that influence the physics of FIB etching are: (1) the dwell time t_p, (2) the natural pixel time constant τ_p, (3) the pattern refresh time t_r, and (4) the natural refresh time constant τ_r. To maintain gas-enhanced etching, one must maintain

$$t_r > \tau_r,$$

and

$$t_p < \tau_p.$$

The first inequality means that repeat time between exposures of any given pixel must be longer than the time required to saturate the pixel with fresh etchant. The second inequality means that the beam should not dwell on a given pixel longer than the time needed to remove all of the adsorbed etchant. Typically, $\tau_p \sim 10$ μs and $\tau_r > 10$ ms (Ref 10). Rue et al. demonstrated the first inequality, referring to τ_r as the pattern loop time (Ref 2). For this work, the first inequality was maintained at all times.

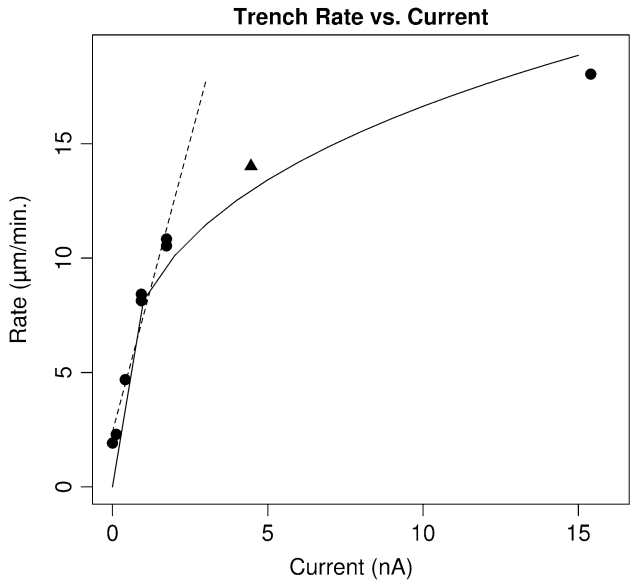

Fig. 8 Trenching rate vs. beam current

Figure 7 shows the trenching rate versus the area for a 50 μm by 50 μm trench, a 4.4 nA beam, 0.4 μm for both px and py, t_p = 0.5 μs, and t_r = 8 ms. The trend shows that fairly large increases in the area have only a small effect on the overall trench rate when working in a gas-enhanced etching mode.

Figure 8 shows a plot of the trenching rate versus the beam current. In all cases, the trenching parameters were a 50 μm by 50 μm box, a pixel spacing of 0.4 μm in x and y, t_p = 0.5 μs,

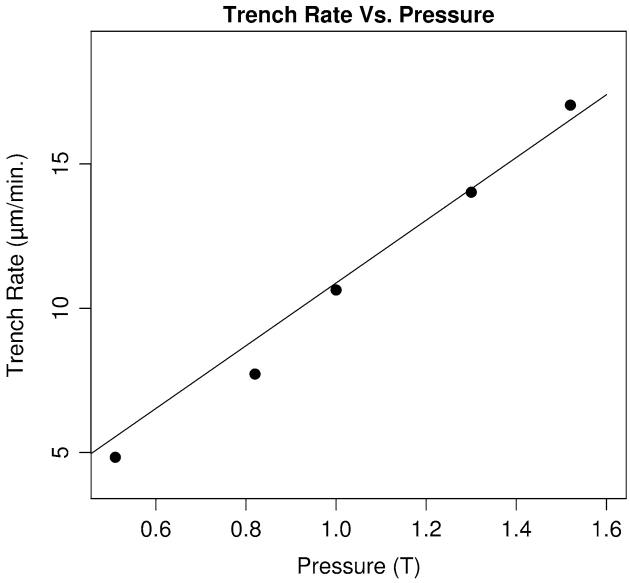

Fig. 9 Trenching rate vs. beehive pressure

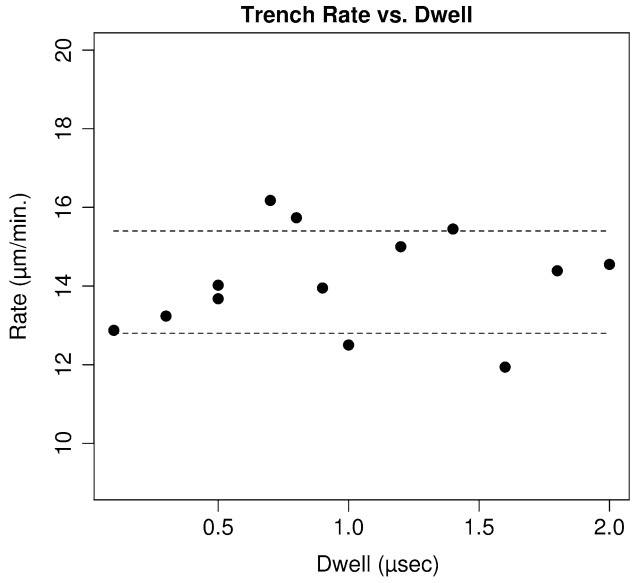

Fig. 10 Trenching rate vs. dwell time

t_r = 8 ms, and a reservoir gas pressure of 1.3 Torr. The curve is a power law fit to the data but otherwise has no physical meaning. The plot shows two clear regimes of operation: (1) a linear region between 0 and 1 nA shown with a dashed line and (2) a non-linear, high-current region between 1 and 15.4 nA.

In the linear region the data fit well to the equation $y = mx + b$ with m = 5.1 µm/min per nA and b = 2.4 µm/min. The y-intercept of 2.4 µm/min compares well with the measurement of 2.55 µm/min in Fig. 4. The data of Fig. 8 shows that increasing the beam at low currents (<1 nA) directly increases the trenching rate. This law fails at higher beam currents. Increasing the beam from 4.4 to 15.4 nA, which is a multiplier of 3.5, increases the trenching rate by only 29% from 14 to 18 µm/min. The high current region is characteristic of a gas depletion mode where t_p exceeds τ_p.

Figure 9 shows the trenching rate versus reservoir gas pressure for a 4.4 nA beam with a pixel spacing of 0.4 µm in both px and py, a milling box of 50 µm by 50 µm, and t_p = 0.5 µm. This condition is the triangular data point shown in Fig. 8. The data fit to the equation $y = mx$ with m equal to 10.9 µm/min/Torr, consistent with Eq (17) of Harriott's digital scan model predicting the trenching rate to be proportional to the gas pressure (Ref 10).

At a reservoir pressure of 1.5 Torr, the chamber pressure rises above 3×10^{-5} Torr where the pressure sensor may trip and shut down the Vectra Vision. Since Fig. 8 shows that at a reservoir pressure of 1.3 Torr gas depletion begins at a 1 nA beam, one could guess that a 4× increase in beam to 4 nA would require a 4× increase in reservoir pressure to 5.2 Torr. This regime is impossible at room temperature since XeF_2 has a vapor pressure of only 4.5 Torr.

Increasing the gas pressure above 49 mTorr in the beehive can also lead to a high pressure effect of increased scattering of the Ga^+ beam. The velocity of Ga^+ ions at 50 KeV is 3.7×10^5 m/s whereas the XeF_2 molecules move at only 210 m/s at 300 °K (Ref 9). The XeF_2 molecules are effectively frozen in position. If one models a column in the beehive with dimensions 100 µm by 100 µm and 2 mm tall, the number of XeF_2 molecules at a pressure of 49 mTorr is 1.5×10^{10}. If each molecule has a cross section of 2.3×10^{-19} m^2, the total cross section for scattering is on the order of $(2.3 \times 10^{-19}\ \text{m}^2) \times (1.5 \times 10^{10}) = 3.5 \times 10^{-9}$ m^2. The probability of scattering is then $(3.5 \times 10^{-9}\ \text{m}^2)/(10^{-8}\ \text{m}^2) = 35\%$. Increasing the gas pressure much beyond 49 mTorr may make the gas opaque to the Ga^+ beam and thwart the trenching process.

Figure 10 shows the trenching rate versus the dwell time. The reservoir gas pressure was held at 1.3 Torr, and the beam parameters were 4.4 nA, 0.4 µm in px and py, and a 50 µm by 50 µm trench (the triangular point in Fig. 8). The removal rate is 14.1 µm/min and independent of t_p. This result shows that dwell time t_p has not been decreased enough to leave the regime of $t_p > \tau_p$. Equation (17) from digital scan model would predict an etch rate independent of the dwell time in this regime as seen in Fig. 10 (Ref 10).

Increasing the pixel spacing, px and py, while holding other parameters constant had no direct effect on the trenching rate. The interpretation within the digital scan model is that controlling factor is the difference between t_p and τ_p, not the spacing between pixels.

Small biases (1 V) on the sample capable of attracting charged particles in the XeF_2 gas to the surface also had no influence on the trenching rate. This result corroborates the results of Houle et al., who showed that n-type and p-type Si etch differently on a quantitative scale not explainable by field effects (Ref 3).

Temperature is an easily variable parameter that affects all processes requiring activation energies. XeF_2 etches Si five times faster at −123 °C than at room temperature, and twice as fast at 327 °C than at room temperature (Ref 11-13). Unfortunately, the expansion coefficient of Si (2.6×10^{-6}/°C) as well as the instability in the sample stage with heating and cooling is not necessarily amenable to circuit modification.

4. Conclusions

The full-thickness backside circuit editing methodology described here is the standard process at Avago Technologies

for the 90/65/40 nm technology arenas. Although trenching through 770 mm of bulk Si increases the time for a circuit edit, the bulk of this added time is returned by avoiding capacitor removal and polishing, and by preventing the waste of time and resources when thinned parts on SLC™ packages crack. The typical time to expose the desired active area and protect the remainder of the trench floor in preparation for a circuit edit is 4 h, a time competitive with a part-thinning process.

Primary levers for increasing the trenching rate are the gas pressure and the beam current. Levers that have little effect as long as they stay within the bounds outlined in the digital scan model include the pixel dwell time, the pixel spacing, and the pattern refresh time (Ref 10). Increasing the primary levers substantially would require tool modification.

Avago chip designers clearly prefer full-thickness backside editing since parts more closely resemble the desired final product. In several high-profile FIB circuit edits, full-thickness parts were mounted onto boards and run at full operating conditions for detailed testing. Parts ran for three weeks without failure, finally ending with the parts still fully functional. In addition to being competitive, the full-thickness backside process has contributed the success of the design team by eliminating risks and uncertainties associated with the part-thinning process.

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